Please replace the paragraph at page 5, lines 18-24, with the following text:

A2

Herein, a stacked capacitor SC corresponding to the position check mark MK2 in the element formation region SR of Fig. 42 will be discussed with reference to Fig. 47. As shown in Fig. 47, the stacked capacitor SC consists of a contact hole 708 selectively so formed as to penetrate the interlayer insulating film 717 and the insulating film 726, a bottom storage node 733 so provided as to fill the contact hole 708, a storage node core 734 formed on the bottom storage node 733 and the sidewall 735 so formed as to surround the storage node core 734.

Page 20, between lines 12 and 13, please insert the following new paragraph:

A3

A more complete appreciation of the present invention and many of the attendant advantages thereof will be readily obtained as the same becomes better understood by reference to the following detailed description when considered in connection with the accompanying drawings, wherein:

Please replace the paragraph at page 23, lines 8-12, with the following text:

A4

The mark structure 100 substantially has the same structure as a gate of an MOS transistor, for it is concurrently formed through the same manufacturing process steps as the gate of the MOS transistor when the MOS transistor is formed as one of semiconductor elements in the element formation region (see Fig. 42), but the mark structure 100 has no function of gate. Therefore, the mark structure 100 is a dummy gate.

Please replace the paragraph at page 24, lines 6-11, with the following text:

A5 cont

Since the bit line layer 113 is formed along an outline of the mark structure 100, covering an upper portion of the interlayer insulating film 107, a side surface of the interlayer insulating film 107 defining the opening 108 and the silicon substrate 101 at the bottom of the opening 108, the level difference of the mark structure 100 is left as a projection and

A6 end

depression of the bit line layer 113 and the mark structure 100 can be measured indirectly through the bit line layer 113.

Please replace the paragraph at page 25, lines 7-18, with the following text:

A4

First, a silicon oxide film serving as the gate oxide film 102 of Fig. 3 is formed on the silicon oxide film 101 to have a thickness of 10 nm, and a polycide layer serving as the gate wiring layer 103 is formed by layering a doped polysilicon layer having a thickness of, e.g., 100 nm and a tungsten silicide layer having a thickness of 100 nm. A TEOS oxide film serving as the insulating film 104 is formed on the polycide layer to have a thickness of, e.g., 200 nm, and a resist mask formed over the TEOS oxide film is selectively etched to form the insulating film 104. After that, using the insulating film 104 as a mask, the lower layers are selectively etched. Subsequently, a TEOS film is formed entirely to have a thickness of, e.g., 50 nm and the TEOS oxide film is so selectively etched as to be left only on side surfaces of the insulating film 104, the gate wiring layer 103 and the gate oxide film 102, to form the sidewall 105. Thus, the mark structure 100 is formed.

Please replace the paragraph at page 25, line 23, through page 26, line 2, with the following text:

A7

Subsequently, in a step of Fig. 4, a resist 210 is so patterned on the interlayer insulating film 107 as to remove the interlayer insulating film 107 in a portion where the mark structures 100 are formed. Then, with the resist 210 as a mask, the interlayer insulating film 107 is selectively removed by dry etching or the like to form the opening 108.

Please replace the paragraph at page 26, lines 9-11, with the following text:

A8

An etching of the stopper insulating film 106 is made under a condition such that the silicon substrate 101 is etched as little as possible, such as by dry etching with CF_4 or the like as the etching gas.